Design of a low voltage,low drop-out (LDO) voltage cmos regulator

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Abstract-

 In this paper a low voltage, low drop-out (LDO) voltage regulator design procedure is proposed and implemented using 0.25 micron CMOS process. It discusses a 3 to 5V, 50mA CMOS low drop-out linear voltage regulator with a single compensation capacitor of 1pF. The experimental results show that the maximum output load current is 50mA and the regulated output voltage is 2.8V.The regulator provides a full load transient response with less than 5mV overshoots and undershoots. The active layout area is 358.28um × 243.30um.

Index Terms: low drop-out, low-voltage regulators, CMOS, linear regulator, power supply circuits, regulators.

I. INTRODUCTION

A Low-drop-out (LDO) regulator is a DC linear voltage regulator which can operate with a very small input-output differential voltage. The demand for the low-voltage, low drop out (LDO) regulators is increasing because of the growing demand of portable electronics, i.e., mobile phones, pagers, laptops, etc as well as industrial and automotive application [1]. Most recently this increasing demand for portable and battery operated products have forced these circuits to operate under low voltage conditions. Furthermore high current efficiency has also become necessary to maximize the lifetime of battery [1]. The regulator should also have a small active area.

LDO design has become more challenging due to the increasing demand of high performance LDO's, of which low-voltage fast-transient LDO's are especially important [1]. Methods to improve the classical LDO structure have been proposed. However, structural limitation, which is the main obstacle in simultaneously achieving stability, high output-voltage accuracy and short response time, still cannot be overcome [2]. The structural limitation of the classical LDO's is mainly due to the associated single pole-zero cancellation schemes, in which an off-chip capacitor with a high equivalent series resistance (ESR) is required to achieve low-frequency pole-zero cancellation.

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The resultant loop gain is not sufficiently high to achieve good line and load regulations and the loop-gain bandwidth is also not sufficiently wide for short response time. In addition, the required high ESR introduces undesirable responses. Low-voltage design is also limited by the voltage buffers inside the classical LDO's [3]. Further improvement on the classical structure is difficult due to the constraint of LDO stability.

Therefore, to achieve good specifications, a novel LDO with a very simple circuit structure is employed. The structure has a double pole-zero cancellation scheme, and the design provides good performance but there is a trade off in settling time.

II. LOW – DROP OUT REGULATOR STRUCTURE AND SCHEMATIC DESIGN

The Structure of the proposed LDO is shown in figure 1. It is composed of two stages. The 1st stage, as in the classical LDO, is the error amplifier use to provide error signal for voltage regulation. And the second stage is a common source amplifier which has a high output swing. Due to cascade architecture, the loop gain depends on the products of the voltage gains of the two gain stages. The high loop gain provides good line and load regulations [1].
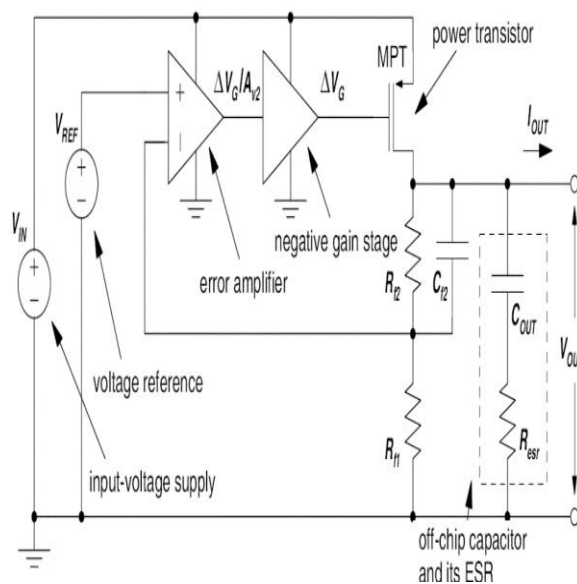

Fig. 1: circuit diagram of proposed LDO regulator

The circuit schematic in figure 2 shows that the error amplifier is a differential pair (M2 & M3) with active load (M4 & M5), while the second gain stage is a common source stage (M6) with a bias – current source (M7). The output swing of the second stage is much better than the source follower in turning on or off the power transistor, and therefore this configuration is suitable for low-voltage LDO designs. The current mirrors (M1, M7 & M8) provide current bias for both the stages.

The power transistor (MPT) is designed to operate in saturation region at drop out. Although the voltage gain of the power transistor is less than unity, the loop gain is not degraded due to the error amplifier and the second gain stage. A loop gain of more than 60dB can be easily achieved in the proposed design and is sufficient for good line and load regulations [1]. In the proposed design for the good transient response performance reason, the transistor size reaches millimeter or even centimeter orders, which generates a bigger gate capacitors. The slew rate at the gate of the power transistor and the frequency response of the LDO disadvantages for the proposed LDO.

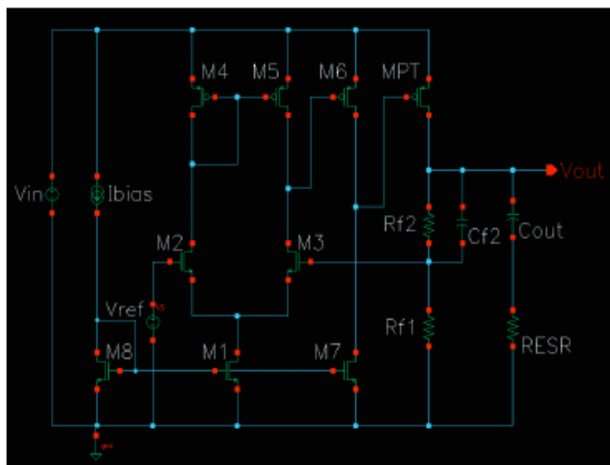Vin works from 3V to 5V, which is the proposed LDO's regulating range.

Fig. 2: Schematic of the proposed LDO regulator

A. DESIGN OF LDO REGULATOR

Design of LDO can be subdivided into the design of power transistor (MPT) and design of two stage op-amp.

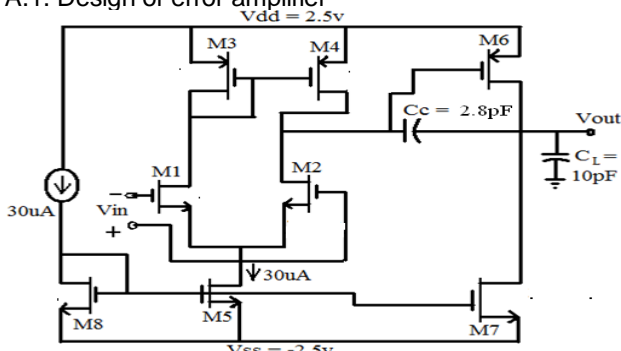A.1. Design of error amplifier

Fig. 3: Schematic of the error amplifier

In this section, a procedure is developed that will enable a first-cut design of the two-stage op-amp. The hand calculation approaches 70% of the design process. The two stage op-amp is designed for the following specs.

TABLE I: Specification for the design of two stage op-amp

Parameter	Parameter Symbol	Quatity
Op amp gain	Av	≥2220V/V
Gain bandwidth	GB	5MHz
Power dissipation	Pdiss	≤1.2mW
Load capacitance	CI	10pf
Slew rate	SR	≥10v/us
Output voltage range	Vout	±2v
Input common mode range	ICMR	-2.5v to +2.5v
Positive voltage	Vdd	+2.5v
Negative voltage	Vss	-2.5v

In order to simplify the the notation, it is convenient to define the notation $S_i = W_i/L_i = (W/L)_i$, where S_i is the ratio of W and L of the i th transistor. We assume that $g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$.

The first step is to calculate the minimum value of the compensation capacitor C_C, it was shown that placing the output pole P_2 2.2 times higher than the GB permitted a 60 phase margin (assuming that the RHP zero Z_1 is placed at or beyond ten times GB). It was shown that such pole and zero placements result in the following requirement for the minimum value for Cc :

$$Cc = 0.22 X C_L$$

$$= (2.2 / 10)*10p = 2.2pF \approx 3pF \qquad (1)$$

Next determine the minimum value for the tail current I_5 , based on slew-rate requirements.

$$I_5 = SR(Cc)$$

$$= 10 * 10^6 *3p$$

$$= 30\mu A \qquad (2)$$

The aspect ratio of M3 can now determined by using the requirement for positive input common-mode range.

$$S_3 = (W/L)_3 = \frac{I_5}{(K_3')[\, V_{dd}- V_{in(max)} - |V_{T03}|_{(max)} + V_{T(min)}]^2}$$
$$= 15$$
$$S4=S3 \qquad (3)$$

Requirements for the transconductance of the input transistors can be determined from knowledge of Cc and GB. The transconductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GB * (Cc)=94.24\mu s$$
(4)

The aspect ratio $(W/L)_1$ is directly obtainable from gm1 as shown below:

$$S_1 = (W/L)_1 = S_2 = \frac{g_{m1}^2}{(K_1')(I_5}$$
$$= 3 \qquad (5)$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship shown:
$$V_{DS5} = V_{in(min)} - V_{ss} - (\underline{I_5})^{1/2} - V_{t1(max)}$$
$$(\beta_1)$$
$$= 0.35V = 350mV \qquad (6)$$

With V_{DS5} determined, $(W/L)_5$ can be extracted using the following way:

$$S_5 = \frac{2I_5}{K_5'(V_{DS5})^2}$$
$$= 4.5 \qquad (7)$$

At this point, the design of the first stage of the op amp is complete. We next consider the output stage. For the phase margin of 60, the location of the output pole was assumed to be placed at 2.2 times GB then zero is placed at least ten times higher than the GB. The transconductance gm6 can be determined using the following relationship:
$$g_{m6} \geq 10g_{m1}$$

$$= 942.4\mu s \qquad (8)$$

so for reasonable phase margin, the value of g_{m6} is approximately ten times the input stage transconductance g_{m1}. At this point, there are two possible approaches to completing the design of M6 (i.e., W_6/L_6 and I_6). The first is to achieve proper mirroring of the first-stage current-mirror load of (M3 and M4). This requires that $V_{GS4} = V_{GS6}$ then:

Assuming g_{m6} = 942.4 µs and calculating gm4 as 10 * 5M * 3p = 150 µs, we use equation to get

$$S_6 = S_4 * \frac{g_{m6}}{g_{m4}}$$

$$= 94 \qquad (9)$$

Knowing g_{m6} and S_6 will define the dc current I_6 using the following equation:

$$I_6 = \frac{g_{m6}^2}{2* (K_6')(W/L)_6}$$

$$= 198.14 \text{ µA}$$
$$(10)$$

The device size of M7 can be determined from the balance equation given below:

$$S_7 = (W/L)_{7 =} (W/L)_5 * (I_6/I_5)$$

$$= 14$$
$$(11)$$

Let us check the Vmin(out) specification although the W/L of M7 is large enough that this is probably not necessary. The value of Vmin(out) is :

$$V_{min(out)} = V_{DS7(sat)} = \sqrt{(\, (2*I6)/(K7*s7))}$$

$$=0.351V \qquad (12)$$
Which is less than required. At this point, the first-cut design is complete.
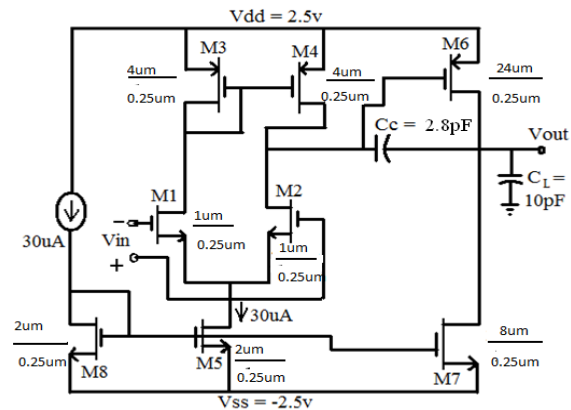

Fig. 4: design of two stage op amp

A.2 Design of MPT stage

Below are the design steps for of power transistor stage

TABLE II. Design specification of power transistor

Parameter	Parameter symbol	quantity
Length	MPTL	2.5µm
Width	MPTW	0.625um
Multiplication Factor	MPTM	3000
Reference voltage	Vref	0.93V
Output capacitance	Cout	20µf
Bias resistance	Rf1	50kΩ
Bias resistance	Rf2	100kΩ
Bias capacitance	Cf2	1pf
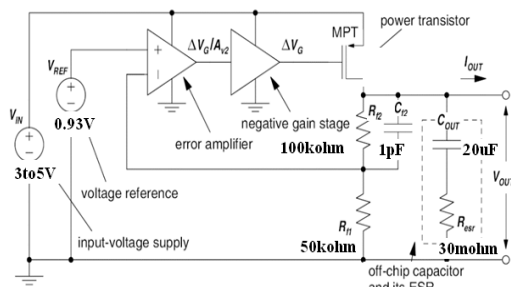
Fig. 5: complete design of power transistor(MPT) stage

The output accuracy of the proposed LDO is high with regard to the effect of the offset voltage since there are only two pair of devices that require good matching(M2-M3 and M4-M5). The offset voltage due to large variations at the error amplifier

Output, occurring in the classical LDOs, is reduced in the proposed LDO due to the gain stage formed by M6 and M7.

Due to the simple circuit structure, the output noise of the proposed LDO is low. Moreover, there is no embedded capacitor or resistor to create poles and zeros for stability purpose, and therefore no coupling noise is imposed on the Error amplifier. Moreover, the output noise from the error amplifier can be minimised by large gm2 and gm3.

III. EXPERIMENTAL RESULTS

The proposed LDO is designed using 0.25µm CMOS technology. The whole chip layout view is shown in figure 13,

And the area is only 359.28µm ×243.3µm. the LDO is capable of operating from 3V to 5 V, which covers a wide range of the typical battery voltage. A dropout voltage of 200mV at a 50mA maximum load current is achieved.

Figure 6 shows the input/output characteristics of the 2.8V LDO regulator. LDO output voltage starts stabilizing at 2.8V when input voltage is 3V. The dropout voltage of LDO is 200mV(3V-2.8V) at 50mA.
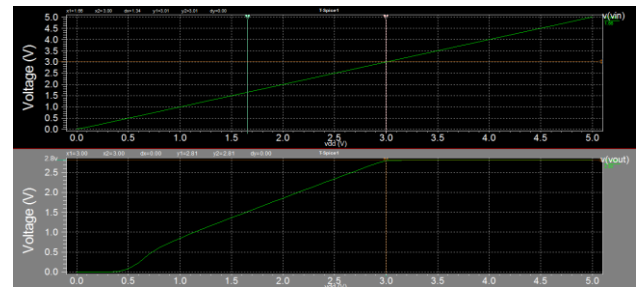

Fig. 6: drop out voltage

An input voltage of 3V and bias current of 30uA is applied to the LDO. Quiescent current is observed to be 129µA as shown in figure 7.
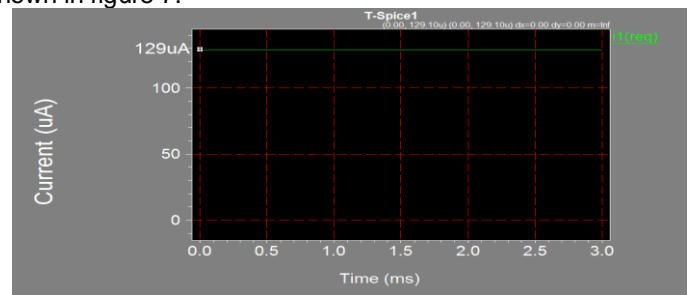

Fig. 7: quiescent current

Owing to the high loop gain provided by the design structure and extremely large size of the transistor, both line and load measurement is pretty good. The measured line and load regulations are 1.85mV/V and 56.4µV/mA as shown in figure 8 and figure 10.
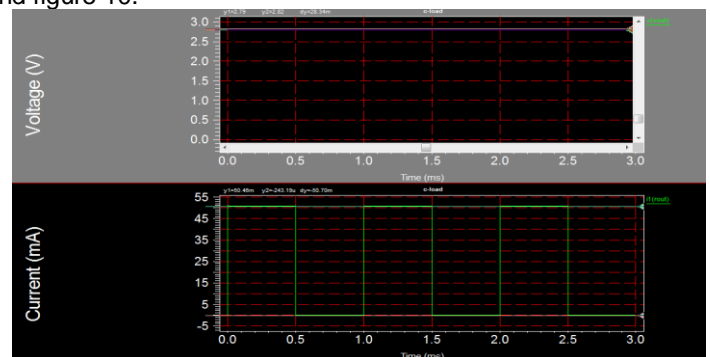

Fig. 8: line regulation

Load regulation of the LDO is measured by NMOS load used as switch with 1ms time period to draw 50mA current when ON and 0mA current when OFF. Vin maintained constant of 5V DC.
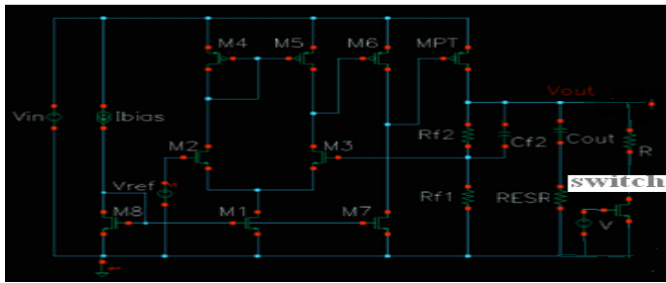
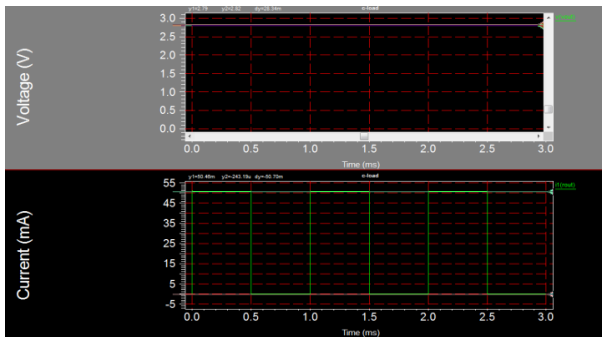Fig 9: LDO with NMOS switch as load

Fig. 10: load regulation

The transient response is 44.53µs. power supply rejection is -68.35dB when operating at 3V.
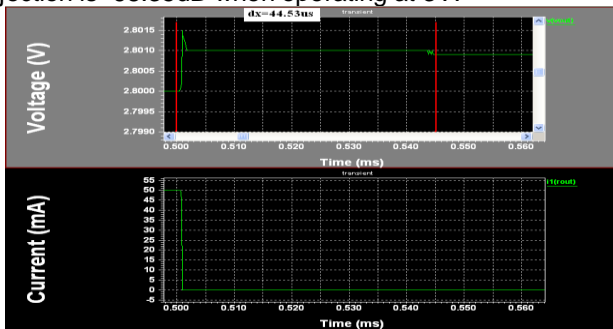

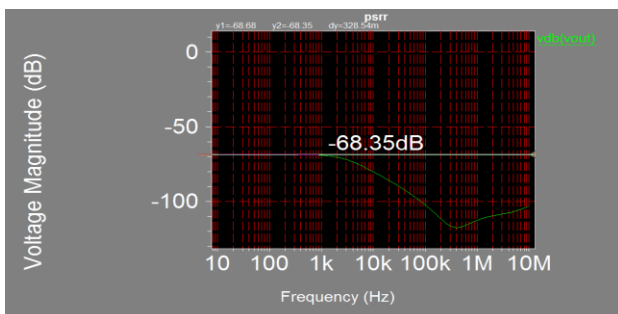Fig.11: full load transient response

Fig.12: PSRR of proposed LDO

As shown in figure 13 gain of the LDO is constant at 55.03dB. the phase at 438.7kHz is 64.13º.
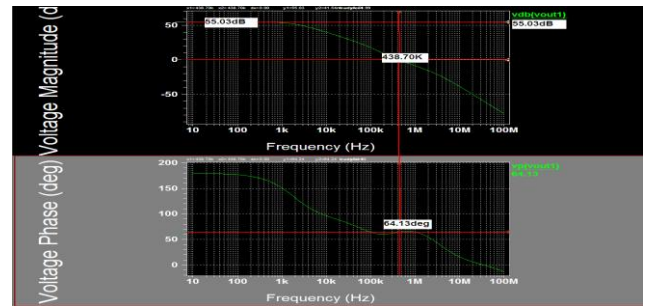

Fig. 13: gain and phase margin of the LDO

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows:

$$\text{Efficiency at 3V input} = ((I0*V0)/((I0+Iq)*Vi)) *100$$
$$= 93.09 \% \qquad (13)$$

Efficiency at 5V input= 55.85%

Where I0 and V0 are current and voltage respectively. Iq is quiescent current.

TABLE III. Summary of measured performance

Technology	0.25µmCMOS
Supply voltage	3V to 5V
Quiescent current	129µA
Output current	50mA
Dropout voltage	200mV
Present output voltage	2.8V
Line regulation	
Load regulation	1.85mV/V
Full load transient response	56µV/mA
	44.34µs
Phase margin	
PSRR	
efficiency	64.13º
	-68.35dB
	93.09% at 3V
	55.85% at 5V

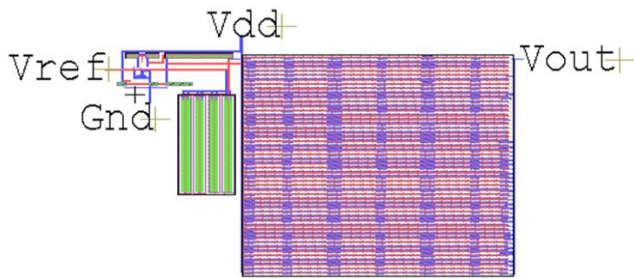The layout of the LDO circuit is given in figure 14.

Fig. 14: proposed LDO full chip layout view

III. CONCLUSION

A low drop out regulation with a compensation capacitor has been proposed. The design is based on a simple but advanced structure ad proposes a double pole-zero cancellation schemes. It meets most of the typical specifications of a commercial LDO. Experimental results show that proposed LDO has small overshoots and undershoots while having excellent line and load regulations. However the proposed design has the disadvantage of slow load transient response. The designed LDO is suitable for powering up low-voltage CMOS mixed-signal systems that require high precision supply voltage as well as low recovery speed.

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